Possible formation of interlayer nano-*p*-*n* junctions and quantum dot in double-walled carbon nanotube with electrode contacts to different layers

T. Shimizu,[1] J. Haruyama,[1,2,3,a)] K. Nozawa,[1] T. Sugai,[4,3] and H. Shinohara[4,3]
[1]*Aoyama Gakuin University, 5-10-1 Fuchinobe, Sagamihara, Kanagawa 229-8558, Japan*
[2]*Institute for Solid State Physics, University of Tokyo, Kashiwanoha 5-1-5, Kashiwa, Chiba 277-8581, Japan*
[3]*JST-CREST, 4-1-8 Hon-machi, Kawaguchi, Saitama 332-0012, Japan*
[4]*Nagoya University, Furo-cho, Chigusa, Nagoya 464-8602, Japan*

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We report findings on the asymmetrical current properties on both the source-drain and back-gate voltage (V_{BG}) dependence (unconventional ambipolar behavior) found in a double-walled carbon nanotube (DWNT) field-effect transistor, which has electrode contacts to different layers. We also find Coulomb oscillations with a large charging energy observable only in $+V_{BG}$ region at low temperature. As origins for these phenomena, we discuss the possible presence of outer *p*- and inner *n*-type semiconducting layers, a corresponding interlayer nano-*p*-*n* junction, and a small quantum dot region in the inner *n*-layer exposed from the outer layer. Annealing of the DWNT in air atmosphere after synthesis allows change in only outer layer to *p*-type, remaining *n*-type behavior in the inner layer. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3108086]

Carbon nanotubes (CNTs), which are typical one-dimensional molecular conductors, have attracted large attention. Conventionally, the structures are classified into two types: (1) single-walled CNTs (SWNTs) and (2) multiwalled CNTs (MWNTs). On the other hand, double-walled CNTs (DWNTs) that comprise only two graphene layers have recently attracted considerable attention.[1–10]

From the viewpoint of physics, a DWNT allows the evident investigation of the interlayer interaction depending on chiralities and diameters.[6–9] From the viewpoint of applications to nanoelectronics, a DWNT can be used to manufacture self-organized nano-Schottky junctions wherein one layer exhibits a semiconducting behavior and the other exhibits a metallic one and also nano-*p*-*n* junction devices wherein one layer exhibits a *p*-type semiconducting behavior and the other does an *n*-type one. These behaviors are expected to be of significance in CNT-LSI circuits as well as in future Si-based LSIs hybridized with CNTs and also nano-photo emission devices.

However, a few researchers have reported experimental observations on electron transport and quantum phenomena in DWNTs. In particular, the interlayer interactions should be highly sensitive to the interlayer current path, which depend on places of the electrode contacts to the two layers. Only in the case of formation of electrode contacts to different layers that interlayer current flow can appear. In turn this current feature can provide information about the interlayer electrical interaction and its applications.

The experimental setup for the preparation of DWNTs has been described in details in Refs. 1–3. High-resolution TEM image of the DWNT is shown in Fig. 1(a). The inset of Fig. 1(a) shows an AFM image of a FET using isolated one DWNT as the current channel. For fabricating FET electrodes, conventional lithography method was used after dispersion of DWNTs on Si substrate with surface SiO_2 layer of 100 nm thickness, except for the following one process. We irradiated electron beam to only one end portion of the DWNT for longer time. This resulted in destruction of the end portion of only the outer layer of the DWNT. It is well known that individual layers of MWNT can be easily destroyed one by one by applying high voltages, electron beam, and other damages.[12] Then, we formed source electrode on this inner layer and drain electrode on the outer layer of the DWNT, as shown in Fig. 1(b). This allows the presence of small inner *n*-layer, which is not surrounded by the outer *p*-layer, and the region might act as a quantum dot, as shown in Fig. 1(b). Because of the above-mentioned electrode contacts, source-drain current (I_{SD}) can flow between the outer and inner layers through the best alignment part of carbon atoms near the end of the outer *p*-layer.

Figure 2(a) shows the I_{SD} as a function of the source-drain voltage, V_{SD} at back-gate voltage, $V_{BG}=0$ V for various temperatures (T). It implies an asymmetric I_{SD} property on applied $\pm V_{SD}$. Such an asymmetric behavior of I_{SD} has not been reported previously. The I_{SD} increases monotonically in both $\pm V_{SD}$ regions as the temperature increases. As shown in Figs. 2(c) and 2(d), they follow thermal-activated-type relationships with activation energies of $\Delta E = \sim 3.4$ and ~ 1.7 meV at $V_{SD}=+0.4$ and -0.4 V, respectively.

Figure 2(b) shows the I_{SD} as a function of V_{BG} at $V_{SD}=+0.4$ V for various T values. It exhibits the so-called ambipolar behavior in the I_{SD} property on $\pm V_{BG}$ at $T=160$ K.

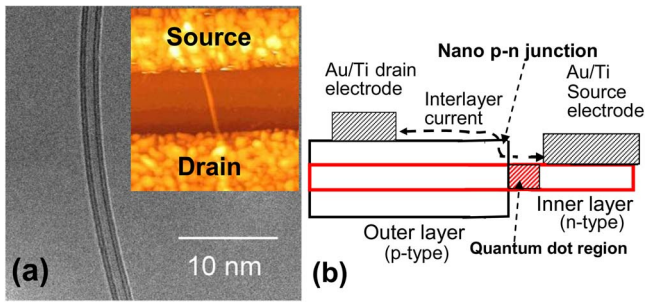

FIG. 1. (Color online) (a) TEM image of DWNT. Inset: AFM images of isolated one DWNT located between source (S) and drain (D) electrodes with 800 nm spacing in a FET. (b) Schematic cross section of the FET with electrode contacts to different layers.

a)Electronic mail: J-haru@ee.aoyama.ac.jp.

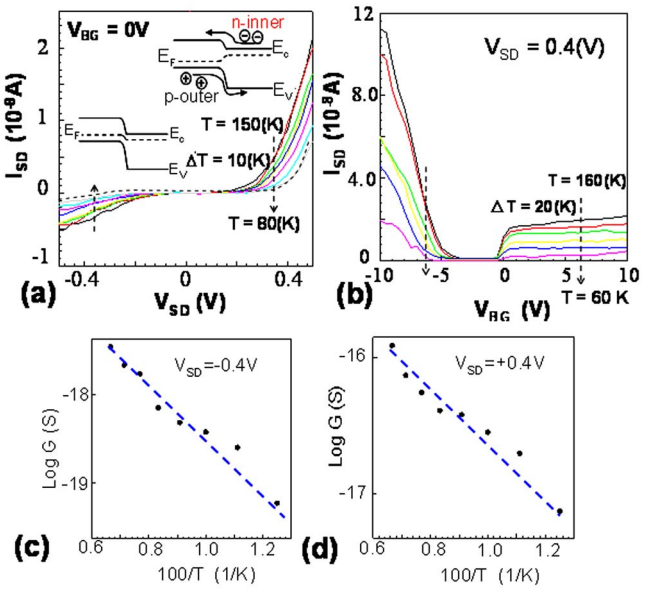

FIG. 2. (Color online) I_{SD} as functions of (a) V_{SD} and (b) V_{BG} for various temperatures. Dotted line in (a) is a calculation result based on Eqs. (1) and (2). Insets of (a): schematic views of band structures in forward (+) and reverse (−) V_{SD} regions (right and left, respectively). [(c) and (d)] Thermal-activation-type relationship in conductance (G) vs temperature at $\pm V_{SD}$ =0.4 V in (a).

Ambipolar behavior has previously been reported in CNT FETs (i.e., in SWNTs, DWNTs, and also carbon nanoscale peapods). However, the ambipolar behaviors of Fig. 2(b) are very unconventional as follows. (1) The I_{SD} increase very gradually with increasing $+V_{BG}$. (2) In contrast, no I_{SD} is observed for V_{BG}=−3.5−−0.5 V and the I_{SD} drastically increases below V_{BG}=−3.5 V with decreasing V_{BG} resulting in no saturation. These resulted in a strong asymmetry of I_{SD} behaviors on applied $\pm V_{BG}$. I_{SD} also increases in both $\pm V_{BG}$ regions with increasing temperature.

The asymmetric I_{SD} properties on applied V_{SD} conventionally originate from the presence of either a Schottky junction or a *p-n* junction existing in the FETs.[10] It is well known that a Schottky junction exists at the interface of electrodes/CNT in CNT-FETs (i.e., when the outer layer has a semiconducting behavior in the case of DWNTs) resulting in Schottky barrier transistors (SBFET) and an ambipolar behavior in $I_{SD}-V_{BG}$ relationship.[11,13] Applied V_{BG} cannot modulate chemical potential of the CNT channel in the SBFET, unlike MOS structure. However, it is well known that in a Schottky junction, the tunnel current is a dominant factor in the I_{SD} in the reverse-biased voltage region and that it is mostly independent of temperature change.[10] This is not consistent with the large temperature dependence shown in Figs. 2(a) and 2(c), as described above. Moreover, asymmetric I_{SD} behaviors have not been observed in our DWNT-FETs with electrode contacts to only the outer layer at both ends. Furthermore, the ambipolar behaviors, as shown in Fig. 2(b), were different from the conventional ambipolar behaviors as mentioned above. Therefore, we conclude that the asymmetric I_{SD} properties in Fig. 2 are not attributed to the presence of Schottky junctions at electrode/DWNT interfaces, unlike CNT-SBFETs.

In contrast, the presence of a *p-n* junction, as shown in Fig. 1 and the insets of Fig. 2(a), can be the candidate for the asymmetric I_{SD} properties when both layers of a DWNT have semiconducting behaviors. In fact, we could confirm the PL emission from both layers in our DWNT, which implies the presence of energy band gaps. Moreover, importantly, we have annealed the present DWNTs at 500 °C for 1–2 h in air after their synthesis.[1–3] Because Ref. 11 reported that such an annealing changes SWNT to a *p*-type one, the outer layer of the present DWNT can have *p*-type semiconducting behavior. In contrast, because the inner layer is protected by the outer layer and it is also isolated by vacuum in the interlayer space in DWNTs, the *n*-type behavior in the inner layer can be maintained even after annealing. This can result in the formation of the interlayer *p-n* junction and yield the asymmetric I_{SD} properties when one electrode can make contact with the inner layer and the other does the outer one in the present structure.

Here, the I_{SD} property of *p-n* junction can be generally given by the following equations for the three-dimensional (3D) *p-n* structures:[10]

$$I_{SD} = J_s\{\exp(eV_s/kT) - 1\}, \tag{1}$$

$$J_s = \mathrm{T}^{\gamma} \exp(-E_g/kT), \tag{2}$$

where V_S, E_g, and γ are the voltage applied to the junction, energy band gap, and constant, respectively. In forward voltage region, I_{SD} increases with increasing temperature following $I_{SD} \propto \exp\{-(E_g - eV_s)/kT\}$ relationship. Also in reverse voltage region, I_{SD} increases with increasing temperature following $I_{SD} \propto \exp(-E_g/kT)$ relationship. In fact, these behaviors are in qualitatively good agreement with the temperature dependence of Fig. 2(a), as shown in Figs. 2(c) and 2(d), which exhibited 1. Monotonic increases in I_{SD} with increasing temperature following thermal activation-type relationship and 2. I_{SD} increases the ratio on temperature increase in $-V_{BG}$ region larger than that in $+V_{BG}$ region. From Fig. 2(d) and Eq. (2), E_g value can be estimated to be ~17 meV. Moreover, the $I_{SD}-V_{SD}$ feature at T=60 K can be well fitted by Eqs. (1) and (2) using E_g of 17 meV and fitting parameters γ, as shown in the dotted line in Fig. 2(a). Because it is very interesting that 3D *p-n* junction model can be still available for the current nano-*p-n* junction, further analysis is indispensable from this viewpoint.

When we follow the above-mentioned *p-n* junction model which denied a possibility of SBFET structure, the unconventionally asymmetric ambipolar behavior on applied V_{BG}, as shown in Fig. 2(b), can be understood as follows. Figure 2(b) was measured under forward V_{SD} region in *p-n* junction (i.e., V_{SD}=+0.4 V), as shown in the right inset of Fig. 2(a). In general MOS structure, the number of electron in the *n*-type inner layer increases by applying $+V_{BG}$ while the number of holes increases in the *p*-type outer layer by applying $-V_{BG}$. In the present DWNT locating on SiO_2 surface, the outer *p*-layer depletes by applying $+V_{BG}$ and it electrically shields the inner layer. Thus, electron can increase by applying $+V_{BG}$ only at the small inner *n*-layer, where it is not surrounded by the outer *p*-layer around the source electrode, as shown in Fig. 1(b). Therefore, I_{SD} increases very gradually with increasing V_{BG} in $+V_{BG}$ region.

In contrast, I_{SD} disappears for V_{BG}=−0.5−−3.5 V. This means that the above-mentioned small inner *n*-layer is quickly depleted as $-V_{BG}$ is applied and the depletion layer acts as a strong barrier layer for hole current flow. As V_{BG} decreases further and when it becomes below V_{BG}=−3.5 V, V_{BG}-induced holes can overflow the barrier and, thus, I_{SD}

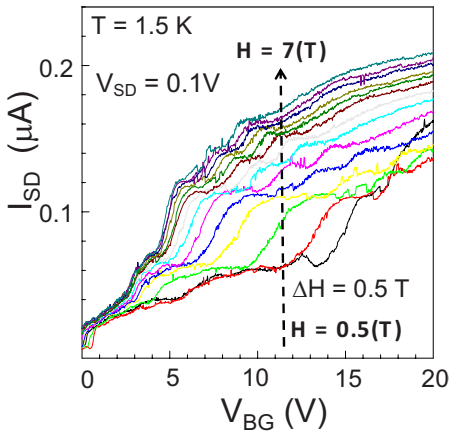

FIG. 3. (Color online) I_{SD} at $T=1.5$ K as a function of V_{BG} for various magnetic fields applied perpendicular to the tube longitudinal axis.

increases drastically. Consequently, this model suggests that the barrier height for holes in valence band at the *p-n* junction is larger than that for electrons in conduction band in built-in potential because electrons can run through the depleted outer *p*-layer at $+V_{BG}$ region. This is attributed to energy band gap of the inner layer larger than that of the outer layer because band gap is inversely proportional to diameter in SWNTs. This also suggests that I_{SD} in Fig. 2(a), which was observed at $V_{BG}=0$ V, is electron current.

Consequently, the unconventionally asymmetric $I_{SD}-V_{BG}$ feature can be interpreted as a result of superposition of the electron and hole currents in the inner *n*-layer and outer *p*-layer, respectively. They originate from the small inner *n*-layer exposed from the outer *p*-layer near source electrode and 2. The barrier heights at *p-n* junction are different for electrons and holes. Moreover, the inner layer is separated from the outer layer by the interlayer spacing of ~0.3 nm, which is larger than those in conventional MWNTs. The large spacing effectively shields the inner layer from the applied $+V_{BG}$. This also induces mostly independent I_{SD} on applied $+V_{BG}$ increase.

All these discussions suggest the presence of the outer *p*-layer and inner *n*-layer and also the formation of the interlayer nano-*p-n* junction in the DWNT-FET. Such a *p-n* junction will exist at the location where the carbon atoms in hexagonal lattices have the highest alignment at the interlayer (i.e., commensurate lattice parts). The above-mentioned discussion suggests that it should be near the end of the outer *p*-layer, as shown in Fig. 1(b).

In order to confirm this model, we performed a single electron spectroscopy by applying V_{BG} in the DWNT at temperature as low as 1.5 K. Figure 3 evidently exhibits staircaselike properties. This is the so-called Coulomb oscillation, which is one of the typical phenomena of SET. SET is based on the charging energy $U_C=e^2/2C$, where C is the capacitance of a quantum dot and also energy spacing between electron orbitals formed in the dot.[14,15] When a magnetic field is applied perpendicular to the tube longitudinal direction, the staircases monotonically shift to the $-V_{BG}$ direction. This implies the absence of electron spin pairs (e.g., spin singlet) and shell filling effect (Zeeman effect) in electron orbitals, unlike quantum dots exhibiting behaviors of artificial atoms. Thus, the Coulomb oscillation originates only from U_C of the present DWNT quantum dot.

Here, it should be noted that the Coulomb oscillation [i.e., Coulomb blockade (CB) region] is observable only in $+V_{BG}$ region. This is consistent with the above-mentioned small inner *n*-layer region, which is not surrounded by the outer *p*-layer, because single electron is injected to the inner *n*-layer from source electrode through a tunnel barrier by applying $+V_{BG}$ at $T=1.5$ K and flows out to the outer *p*-layer through the *p-n* junction. Thus, the small *n*-layer can act as a quantum dot, as shown in Fig. 1(b) and the inset of Fig. 2(a).

We find that the CB region disappears at around $V_{SD}=0.5$ V as V_{SD} increases. We cannot estimate U_C values directly from the Coulomb oscillation periods because the applied V_{BG} is transferred via silicon substrate and cannot directly reflect the U_C values. However, the large CB voltage of 0.5 V implies a $U_C(=e^2/2C)$ value as large as 0.5 eV and also a C value as small as $\sim 10^{-18}$ F. Because the U_C values of conventional SWNT quantum dots with lengths of 100–200 nm are ~25 meV,[15] this U_C value of 0.5 eV in the DWNT suggests that the quantum dot region is as small as 5–10 nm. This is in qualitatively good agreement with the above-mentioned small inner *n*-layer region, which acts as a quantum dot. Moreover, the barrier height for holes in valence band at the *p-n* junction is larger than that for electrons as mentioned above. Hence, a single hole cannot flow into the inner *n*-layer from the *p*-layer. Because the length of the outer *p*-layer is also longer than ~700 nm, it does not act as quantum dot. These are also consistent with the appearance of Coulomb oscillation only in the $+V_{BG}$ region.

However, from the qualitative viewpoint, this size of quantum dot and C value estimated from the large U_C value are too small because such a large U_C value has not been observed in any of our SWNT and DWNT quantum dots with contacts to only the outer layer at both ends, which were fabricated through the same FET process. Hence, it should be unique to the present DWNT quantum dot with electrode contacts with different layers. This might be attributed to electrostatic coupling of the outer *p*-layer to the inner *n*-layer quantum dot in series because the *p-n* junction is within the forward biased in Fig. 3 and the series electrostatic coupling between *p-n* layers is strong.

Although it is essential to reconfirm these conclusions by means of other observations and find further advantages of nano-*p-n* junction, the present results promise the application of DWNTs as self-organized nano-*p-n* junctions to CNT-LSI circuits. Moreover, photoemission devices based on the present interlayer nano-*p-n* junction are highly expected.

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